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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,554	01/23/2004	Hirokazu Honda	NEC 26485	7561

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/763,554	HONDA, HIROKAZU	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *10-15,18 and 19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,16 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/23/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/763554 Attorney's Docket #: NEC 26485
Filing Date: 1/23/2004; priority to 2/3/2003 and 12/10/2003

Applicant: Honda

Examiner: Alexander Williams

Applicant's Amendment filed 2/23/06 to the election of the species I, figures 1a, 1b, 8a-8h and 12a (claims 1-9, 16-18 and 19), filed 9/26/05, has been acknowledged. As of this action, claims 18 and 19 are now withdrawn.

This application contains claims 10-15, 18 and 19 drawn to an invention non-elected without traverse.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 to 6 are rejected under 35 U.S.C. § 102(e) as being anticipated by Gealer (U.S. Patent Application Publication # 2005/0121757 A1).

1. Gealer (figures 1 to 13) specifically figure 3 show a semiconductor device comprising: a semiconductor chip **10** mounted on a mounting substrate **20**; a first resin **30** filling a gap between the semiconductor chip and the mounting substrate; a stiffener **40** surrounding the semiconductor chip; and a second resin **90/95** filling a space between the semiconductor chip and the stiffener in contact with the first resin, the first resin being different in a thermal expansion coefficient from the second resin.

2. The semiconductor device as claimed in claim 1, Gealer show wherein a thermal expansion coefficient of the second resin is smaller than a thermal expansion coefficient of the first resin.

3. The semiconductor device as claimed in claim 2, Gealer show wherein the stiffener is adhered to the mounting substrate with a resin the same as the second resin.

4. The semiconductor device as claimed in claim 1, Gealer show wherein the first resin includes an underfill **30** part filling the gap between the semiconductor chip and the mounting substrate, and a fillet part extended from a region of the semiconductor chip.

5. The semiconductor device as claimed in claim 1, Gealer show wherein the stiffener **40** is adhered to the mounting substrate with a first adhesive **45** being larger in a thermal expansion coefficient than the second resin.

6. The semiconductor device as claimed in claim 4, Gealer show wherein the second resin **90/95** is in contact with inner walls of the stiffener **60**, the fillet part **30**, the mounting substrate **20** and each of side faces of the semiconductor chip **10**.

[0018] Substrate 20 comprises solder balls 25 for carrying power and I/O signals between elements of apparatus 1 and external devices. For example, solder balls 25 may be mounted directly to a motherboard (not shown) or onto an interposer that is in turn mounted directly to a motherboard. Alternative interconnects such as through-hole pins may be used instead of solder balls 25 to mount apparatus 1 to a motherboard, a socket, or another substrate.

[0019] Underfill material 30 encapsulates the electrical coupling between the die and the substrate and may. therefore protect the coupling from exposure to environmental hazards. Underfill material 30 may be used to assist the mechanical coupling between IC die 10 and IC package 20. For example, electrical contacts 15 may experience mechanical stress when heated due to a difference between the coefficient of thermal expansion (CTE) of IC die 10 and the CTE of IC package 20. Underfill material 30 may address this mismatch by distributing the stress away from the connections.

[0020] Stiffener portion 40 may also reduce the mechanical stress experienced by electrical connections 15. Stiffener portion 40 may cause IC package 20 to deform less in response to environmental and operational conditions than IC package 20 would otherwise deform in the absence of stiffener portion 40. According to some embodiments, stiffener portion 40 causes an area of IC package 20 to which IC die 10 is coupled to deform more similarly to IC die 10 in response to certain environmental and operational conditions. Although not apparent from the FIG. 1 cross-sectional view, stiffener portion 40 surrounds IC die 10 according to some embodiments.

[0021] Stiffener portion 40 may comprise any suitable material including but not limited to a temperature-resistant polymer. Stiffener portion 40 is coupled to IC package 20 using adhesive 45. According to some embodiments, stiffener portion 40 is coupled to IC package 20 without the use of adhesive 45.

Stiffener portion 40 may protect the edges of IC package 20, and may provide a contact surface for handling apparatus 1.

[0022] FIG. 2 is a top view of stiffener strip 50 according to some embodiments. Stiffener strip 50 may be comprised of any currently- or hereafter-known suitable material, including those described above with respect to stiffener portion 40. Selection of the material may depend on the particular fabrication process used in conjunction with stiffener strip 50. One such process is described below.

[0035] A top view of a singulated IC die 10 and its respective mounting location of IC package substrate 70 is shown in FIG. 11. The FIG. 11 apparatus is identical to apparatus 1 of FIG. 1 according to some embodiments.

[0036] In some embodiments of process 60, stiffener strip 50 may be placed on IC package substrate before 61, 62, or 63. These embodiments may require a designer to ensure that openings 55 are large enough to allow underfill material to be properly dispensed around IC die 10.

[0037] FIG. 12 illustrates apparatus 80 according to some embodiments. The elements of apparatus 80 may be identical to similarly-numbered elements of apparatus 1. As shown, stiffener portion 40 extends farther from IC package 20 than does die 10. Stiffener portion 40 and IC package 20 thereby define well 90 in which IC die 10 is disposed. According to some embodiments, well 90 is filled with thermally-conductive material 95.

[0038] Moreover, heat sink 100 is coupled to stiffener portion 40 and is in contact with thermally-conductive material 95. Heat sink 100 may comprise any currently- or hereafter-known passive or active heat sink. A thermally-conductive paste or other material may be disposed between thermally-conductive material 95 and heat sink 100, and/or between stiffener portion 40 and heat sink 100. Such an arrangement may improve the conductivity of heat away from die 10.

[0039] FIG. 13 is a cross-sectional side view of system 200 according to some embodiments. System 200 may comprise components of a server platform. System 200 includes apparatus 1 as described above, memory 210 and motherboard 220. Apparatus 1 may comprise a microprocessor.

[0040] Motherboard 220 may electrically couple memory 210 to apparatus 1. More particularly, motherboard 220 may comprise a memory bus (not shown) that is electrically coupled to solder balls 25 and to memory 210. Memory 210 may comprise any type of memory for storing data, such as a Single Data Rate Random Access Memory, a Double Data Rate Random Access Memory, or a Programmable Read Only Memory.

Claims 1 to 4 are rejected under 35 U.S.C. § 102(e) as being anticipated by Pu et al. (U.S. Patent Application Publication # 2002/0121705 A1).

1. Pu et al. (figures 1 to 10) specifically figures 6 and 10 show a semiconductor device comprising: a semiconductor chip **31** mounted on a mounting substrate **30**; a first resin **33** filling a gap between the semiconductor chip and the mounting substrate; a stiffener **(303 or 36)** surrounding the semiconductor chip; and a second resin **35** filling a space between the semiconductor chip and the stiffener in contact with the first resin, the first resin being different in a thermal expansion coefficient from the second resin.

2. The semiconductor device as claimed in claim 1, Pu et al. show wherein a thermal expansion coefficient of the second resin is smaller than a thermal expansion coefficient of the first resin.

3. The semiconductor device as claimed in claim 2, Pu et al. show wherein the stiffener is adhered to the mounting substrate with a resin the same as the second resin.

4. The semiconductor device as claimed in claim 1, Pu et al. show wherein the first resin includes an underfill **33** part filling the gap between the semiconductor chip and the mounting substrate, and a fillet part extended from a region of the semiconductor chip.

Initially, it is noted that the 35 U.S.C. § 103 rejection based on a second resin, a stiffener and (an adhesive or first adhesive) deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Claims 1 to 4, 7 to 9, 16 and 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Akram et al. (U.S. Patent # 5,866,953).

1. Akram et al. (figures 1 to 9) specifically figures 4 and 5 show a semiconductor device **400** comprising: a semiconductor chip **402** mounted on a mounting substrate **416**; a first resin **422** filling a gap between the semiconductor chip and the mounting substrate; a stiffener **(outer portion of 424)** surrounding the

semiconductor chip; and a second resin **(inner portion of 424)** filling a space between the semiconductor chip and the stiffener in contact with the first resin, the first resin being different in a thermal expansion coefficient from the second resin.

[0008] After assembly as shown in FIG. 1, a glob of encapsulant material 102 (usually epoxy or silicone or a combination thereof) is generally applied to a COB assembly 100 to surround a semiconductor chip or flip chip 104 which is attached to a substrate 106 via a plurality of electrical connections 108 which extends between a plurality of semiconductor chip bond pads 110 and a corresponding plurality of substrate bond pads 112. An underfill encapsulant 114 is dispensed between the semiconductor chip 104 and the substrate 106. As shown in FIG. 2, the glob top materials 202 are often used to hermetically seal bare dice 204 (shown in shadow) on a printed circuit board 206 such as SIMM modules to form a COB assembly 200. The organic resins generally used in the glob top encapsulation are usually selected for low moisture permeability and low thermal coefficient of expansion to avoid exposure of the encapsulated chip to moisture or mechanical stress respectively. However, even though the chemical properties of these glob top materials have desirable properties for encapsulation, the thermal and electrical properties are often not optimal for removing heat efficiently away from the semiconductor dice or for use in high temperature areas.

[0030] FIG. 4 illustrates a first encapsulated semiconductor assembly 400 of the present invention. The first encapsulated semiconductor assembly 400 comprises a flip chip or semiconductor chip 402 having a plurality of bond pads 404 on an active surface 406 of the semiconductor chip 402. A facing surface 408 of each bond pad 404 has a conductive pad 410 in electrical communication therewith. The conductive pads 410 are in electrical communication with a plurality of respective bond pads 412 on an upper surface 414 of a substrate 416. Each substrate bond pad 412 is connected on a lower bond pad surface 418 to a trace lead 420 (shown by a dashed line). An underfill encapsulant 422 may be disposed between the semiconductor chip 402 and the substrate 416.

[0031] As seen in FIGS. 4 and 5, a barrier glob top 424 is applied to surround a periphery of the semiconductor chip 402 which seals and protects the semiconductor chip 402 and forms a recess or cavity 426. A heat-dissipating glob top 428 is disposed within the recess 426 as shown in FIG. 4.

2. The semiconductor device as claimed in claim 1, Akram et al. show wherein a thermal expansion coefficient of the second resin is smaller than a thermal expansion coefficient of the first resin.

3. The semiconductor device as claimed in claim 2, Akram et al. show wherein the stiffener is adhered to the mounting substrate **416** with a resin **424** the same as the second resin **424**.

4. The semiconductor device as claimed in claim 1, Akram et al. show wherein the first resin includes an underfill part filling the gap between the semiconductor chip and the mounting substrate, and a fillet part extended from a region of the semiconductor chip.

7. Akram et al. (figures 1 to 9) specifically figures 4 and 5 show a semiconductor device **400** comprising: a semiconductor chip **402** mounted on a mounting substrate **416**; a first resin **422** filling a gap between the semiconductor chip and the mounting substrate; a stiffener **(outer portion of 424)** surrounding the semiconductor chip; a second resin **(inner portion of 422)** filling a space between the semiconductor chip and the stiffener in contact with the first resin, the first resin being different in a thermal expansion coefficient from the second resin; and a lid **428** for covering the stiffener and the semiconductor chip, wherein the lid is bonded to the stiffener and a backside of the semiconductor chip with an adhesive **428**.

8. The semiconductor device as claimed in claim 7, Akram et al. show wherein the second resin is in contact with an inner wall of the lid.

9. The semiconductor device as claimed in claim 1, Akram et al. show wherein an elastic modulus of the second resin is larger than an elastic modulus of the first resin.

16. The semiconductor device as claimed in claim 1, Akram et al. show wherein the stiffener is made of a material selected from the group consisting of Cu, SUS, Al, alumina, silicon, aluminum nitride, and **resin**.

17. The semiconductor device as claimed in claim 1, Akram et al. show wherein each of the first resin and the second resin essentially contains a resin selected from a group consisting of epoxy, polyolefin, silicon, cyanate ester, polyimide, polynorbornene resins.

Therefore, it would have been obvious to one of ordinary skill in the art to use the second resin, the stiffener and the second adhesive as "merely a matter of obvious engineering choice" as set forth in the above case law.

Initially, it is noted that the 35 U.S.C. § 103 rejection based on a second resin and (an adhesive or a first adhesive) deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an

article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

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Claims 7 to 9, 16 and 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Gealer (U.S. Patent Application Publication # 2005/0121757 A1).

7. Gealer (figures 1 to 13) specifically figure 3 show a semiconductor device comprising: a semiconductor chip **10** mounted on a mounting substrate **20**; a first resin **30** filling a gap between the semiconductor chip and the mounting substrate; a stiffener **40** surrounding the semiconductor chip; a second resin **90/95** filling a space between the semiconductor chip and the stiffener in contact with the first resin, the first resin being different in a thermal expansion coefficient from the second resin; and a lid **100** for covering the stiffener and the semiconductor chip, wherein the lid is bonded to the stiffener and a backside of the semiconductor chip with an adhesive **90/95**.

8. The semiconductor device as claimed in claim 7, Gealer show wherein the second resin **90/95** is in contact with an inner wall of the lid **100**.

9. The semiconductor device as claimed in claim 1, Gealer show wherein an elastic modulus of the second resin is larger than an elastic modulus of the first resin.

16. The semiconductor device as claimed in claim 1, Gealer show wherein the stiffener is made of a material selected from the group consisting of **Cu**, SUS, **Al**, alumina, silicon, aluminum nitride, and resin.

17. The semiconductor device as claimed in claim 1, Gealer show wherein each of the first resin and the second resin essentially contains a resin selected from a group consisting of epoxy, polyolefin, silicon, cyanate ester, polyimide, polynorbornene resins.

Therefore, it would have been obvious to one of ordinary skill in the art to use the second resin and the second adhesive as "merely a matter of obvious engineering choice" as set forth in the above case law.

[0035] A top view of a singulated IC die 10 and its respective mounting location of IC package substrate 70 is shown in FIG. 11. The FIG. 11 apparatus is identical to apparatus 1 of FIG. 1 according to some embodiments.

[0036] In some embodiments of process 60, stiffener strip 50 may be placed on IC package substrate before 61, 62, or 63. These embodiments may require a designer to ensure that openings 55 are large enough to allow underfill material to be properly dispensed around IC die 10.

[0037] FIG. 12 illustrates apparatus 80 according to some embodiments. The elements of apparatus 80 may be identical to similarly-numbered elements of apparatus 1. As shown, stiffener portion 40 extends farther from IC package 20 than does die 10. Stiffener portion 40 and IC package 20 thereby define well 90 in which IC die 10 is disposed. According to some embodiments, well 90 is filled with thermally-conductive material 95.

[0038] Moreover, heat sink 100 is coupled to stiffener portion 40 and is in contact with thermally-conductive material 95. Heat sink 100 may comprise any currently- or hereafter-known passive or active heat sink. A thermally-conductive paste or other material may be disposed between thermally-conductive material 95 and heat sink 100, and/or between stiffener portion 40 and heat sink 100. Such an arrangement may improve the conductivity of heat away from die 10.

[0039] FIG. 13 is a cross-sectional side view of system 200 according to some embodiments. System 200 may comprise components of a server platform. System 200 includes apparatus 1 as described above, memory 210 and motherboard 220. Apparatus 1 may comprise a microprocessor.

[0040] Motherboard 220 may electrically couple memory 210 to apparatus 1. More particularly, motherboard 220 may comprise a memory bus (not shown) that is electrically coupled to solder balls 25 and to memory 210. Memory 210 may comprise any type of memory for storing data, such as a Single Data Rate Random Access Memory, a Double Data Rate Random Access Memory, or a Programmable Read Only Memory.

Claims 7 to 9, 16 and 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Pu et al. (U.S. Patent Application Publication # 2002/0121705 A1).

5. The semiconductor device as claimed in claim 1, Pu et al. show wherein the stiffener **(36)** is adhered to the mounting substrate with a first adhesive **35** being larger in a thermal expansion coefficient than the second resin.

6. The semiconductor device as claimed in claim 4, Pu et al. show wherein the second resin **35** is in contact with inner walls of the stiffener **(36)**, the fillet part **33**, the mounting substrate **30** and each of side faces of the semiconductor chip **31**.

7. Pu et al. (figures 1 to 10) specifically figures 6 and 10 show a semiconductor device comprising: a semiconductor chip **31** mounted on a mounting substrate **30**; a first resin **33** filling a gap between the semiconductor chip and the mounting substrate; a stiffener **(303 or 36)** surrounding the semiconductor chip; a second resin **35** filling a space between the semiconductor chip and the stiffener in contact with the first resin, the first resin being different in a thermal expansion coefficient from the second resin; and a lid **36** for covering the stiffener and the semiconductor chip, wherein the lid is bonded to the stiffener and a backside of the semiconductor chip with an adhesive **35**.

8. The semiconductor device as claimed in claim 7, Pu et al. show wherein the second resin **35** is in contact with an inner wall of the lid **36**.

9. The semiconductor device as claimed in claim 1, Pu et al. show wherein an elastic modulus of the second resin **35** is larger than an elastic modulus of the first resin **33**.

16. The semiconductor device as claimed in claim 1, Pu et al. show wherein the stiffener **(303 or 36)** is made of a material selected from the group consisting of **Cu**, SUS, **Al**, alumina, silicon, aluminum nitride, and resin.

17. The semiconductor device as claimed in claim 1, Pu et al. show wherein each of the first resin and the second resin essentially contains a resin selected from a group consisting of epoxy, polyolefin, silicon, cyanate ester, polyimide, polynorbornene resins.

Therefore, it would have been obvious to one of ordinary skill in the art to use the second resin and the second adhesive as "merely a matter of obvious engineering choice" as set forth in the above case law.

Response

Applicant's arguments filed 2/23/06 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/778,737,738,734,787,788,789,790,795,792,793,796,704,706,707,710,712,713,717,720,698,e23.14,e23.092,23.087,e23.19	10/13/05 5/11/06
Other Documentation: foreign patents and literature in 257/778,737,738,734,787,788,789,790,795,792,793,796,704,706,707,710,712,713,717,720,698,e23.14,e23.092,23.087,e23.19	10/13/05 5/11/06
Electronic data base(s): U.S. Patents EAST	10/13/05 5/11/06

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
5/11/06